INTEROFFICE MEMORANDUM

M-1068

DATE January 13, 1960

SUBJECT Complementing Checkerboard Program

TO PDP Distribution List

FROM John C. Conley

This is a utility program for checking the performance and reliability of the magnetic core memory. It works the memory in the roughest way possible and is self-checking for easy location of faulty or weak cores.

The memory is loaded in a fixed order from the test word, using both the test word and its complement.

The content of each register is then checked, and if correct the content is complemented and stored. The program after initial loading is in a continuous loop of checking, complementing, storing and then checking again, complementing and storing. This will continue indefinitely until the machine is stopped manually or on the location of an error during checking.

The memory plane is loaded in the following order, assuming that the test word is all 1's and that the skip instruction in register 1717 is skip on AC positive. This instruction is set by the program and may be a skip on either positive or negative. If negative the loading will be the complement of that shown. Any combination of 1's and 0's may be used in the test word.

MEMORY PLANE

Register	0	1	2	3	4	5	6	7	10	11	12	13	14	15	16	17	20		35	36	37
0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	------	0	0	1
40	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	------	1	1	0
100	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	------			
.	.	.																			
.	.	.																			
.	.	.																			
.	.	.																			
.	.	.																			
1640	0	1																			

1700)
1740) Program is in these registers

OPERATING INSTRUCTIONS

1. Set Test Word to configuration of 1's and 0's you want to use.

2. Set Test Address to 1700.

3. Push start switch on console.

4. The machine will halt at 1745 (PC = 1746) if an error is detected. The AC will show the address of the register containing the error.

5. To locate faulty core, set Test Address to address shown in AC. Push examine switch and locate, core which is incorrect. For example, if 1's and 0's have been loaded, faulty core will have a 1 while the rest of the register shows 0's or just the reverse of this.

6. To determine what should be in any register examine program registers 1717 and 1737. If they are the same memory should contain what was loaded initially, if they are different the program is in the complement cycle and the complement of what was loaded should be in memory.

NOTE: If this examination is made after a halt at 1745, all registers before the address shown in the AC will have been complemented and so be the reverse of the statement above. Those registers after the address in the AC will be as explained above.

COMPLEMENTING CHECKERBOARD

Key	Address	Instruction	Code	Comments
	1700	LAC L	20-1767)	Sets skip instruction for initial load
	1701	DAC D	24-1737)	and check of memory registers 0-1677
	1702	DAC G	24-1717)	
	1703	LAC T	20-1777)	Puts in dummy instruction for initial
	1704	DAC F	24-1716)	loading of memory
E	1705	LAC Z	20-1772)	Designates first register to be loaded
	1706	DAC Q	24-1775)	or checked
A	1707	LAC Q	20-1775)	
	1710	RAR 5	67-1037)	
	1711	XOR Q	06-1775)	Determines what should be in each
	1712	DAC M	24-1770)	memory register
	1713	RAR 1	67-1001)	
	1714	XOR M	06-1770)	
	1715	RAR 1	67-1001)	
F	1716	(Dummy (JMP D	76-000 60-1737	
G	1717	(SPA (SNA	64-----)	
	1720	JMP C	60-1723)	
	1721	LAT	76-2200)	
	1722	JMP B	60-1724)	Loads memory initially
C	1723	LAT & CMA	76-3200)	
B	1724	DAC* Q	25-1775)	
	1725	IDX Q	44-1775)	
	1726	SAS V	52-1771	Checks for last register
	1727	JMP A	60-1707	
	1730	LAC R	20-1774	
	1731	DAC F	24-1716	
	1732	LAT	76-2200)	
	1733	DAC W	24-1776)	Sets constants from TW for checking
	1734	CMA	76-1000)	
	1735	DAC P	24-1773)	
	1736	JMP E	60-1705	Start checking
D	1737	(SPA (SNA	64-0200 64-0400	

Complementing Checkerboard .. cont'd.

Key	Address	Instruction	Code	Comments
	1740	JMP H	60-1746)	
	1741	LAC*Q	21-1775)	
	1742	SAD W	50-1776)	
	1743	JMP J	60-1751)	
N	1744	LAC Q	20-1775)	Checks memory register and reloads
	1745	Halt	76-0400)	complement. If error is detected
H	1746	LAC*Q	21-1775)	halts at 1745 with address of incor-
	1747	SAS P	52-1773)	rect register in AC
	1750	JMP N	60-1744)	
J	1751	CMA	76-1000)	
	1752	DAC*Q	25-1775)	
	1753	IDX Q	44-1775)	Checks for last register
	1754	SAS V	52-1771)	
	1755	JMP A	60-1707	
	1756	LAC K	20-1766)	
	1757	DAC D	24-1737)	
	1760	DAC M	24-1770)	Changes skip instruction after each
	1761	LAC L	20-1767)	complete run through of memory for
	1762	DAC K	24-1766)	next check and complement cycle
	1763	LAC M	20-1770)	
	1764	DAC L	24-1767)	
	1765	JMP E	60-1705	
K	1766	SPA	64-0200	
L	1767	SNA	64-0400	
M	1770			
V	1771		001700	
Z	1772		000000	
P	1773			
R	1774		60-1737	
Q	1775			
W	1776			
T	1777		76-0000	